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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI22-1332
First Inventor or Application Identifier	Honeycutt
Title	Transistor Structures, Methods of...
Express Mail Label No.	EL465687187

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APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [XX] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)
2. [XX] Specification [Total Pages 24] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [XX] Drawing(s) (35 U.S.C. 113) [Total Sheets 9]
4. Oath or Declaration [Total Pages 3]
   a. [XX] UNEXECUTED ~~Newly executed~~ (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed)
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

* NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
9. [ ] English Translation Document (if applicable)
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [XX] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
13. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
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16. **If a CONTINUING APPLICATION,** check appropriate box, and supply the requisite information below and in a preliminary amendment:
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Prior application information: Examiner ______ Group / Art Unit: ______

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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Transistor Structures, Methods of Forming Transistor Structures, and Methods of Forming Insulative Material Against Conductive Structures

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ATTORNEY'S DOCKET NO. MI22-1332

Transistor Structures, Methods of Forming Transistor Structures, and Methods of Forming Insulative Material Against Conductive Structures

TECHNICAL FIELD

The invention pertains to methods of forming insulative materials against conductive structures, and in particular aspects pertains to methods of forming transistor structures. Also, the invention pertains to transistor structures.

BACKGROUND OF THE INVENTION

A frequently used procedure of semiconductor fabrication is formation of a so-called "self-aligned contact" (SAC) opening. An exemplary use of a SAC opening is to expose a node between a pair of wordlines, and can be conducted as follows. First, a pair of adjacent wordlines are formed over a substrate, and then insulative sidewall spacers are formed along conductive portions of the lines. The wordlines typically comprise conductive portions capped by insulative material. Suitable insulative material for capping the wordlines is silicon nitride. A thick insulative layer (typically borophosphosilicate glass (BPSG)) is formed over the wordlines and insulative sidewall spacers. The insulative sidewall spacers are formed of a material different than the thick insulative layer, with a suitable material being silicon nitride.

An opening is etched through the thick insulative layer and to an electrical node between the wordlines. If the thick insulative layer

comprises BPSG and the sidewall spacers comprise silicon nitride, the etch utilizes conditions which are selective for the BPSG relative to the silicon nitride. The insulative spacers are exposed during formation of the opening, but are etched more slowly than the BPSG, and preferably are not entirely removed by the etch of the BPSG. The opening is intended to be formed to have a periphery "aligned" with the spacers, and the formation of the opening is referred to as a "self-aligned contact" etch.

It is desired that the spacers not be entirely removed during formation of the opening so that the spacers can protect the conductive material of the wordlines from being exposed when the opening is formed. If the conductive material of the wordlines becomes exposed in the openings, device failure will likely result. A problem with current semiconductor fabrication processes is that silicon nitride insulative spacers are occasionally over-etched during formation of contact openings in BPSG, leading to exposure of wordline conductive material, and to device failure.

A possible method for overcoming the above-discussed problem is described in U.S. Pat. No. 5,700,349, which suggests utilizing $Si_xO_yN_z$ or Al_xO_y based materials to protect conductive portions of a wordline during a SAC method. The utilization of $Si_xO_yN_z$ and Al_xO_y as protective materials relative to the conductive material of a wordline during a SAC method shows promise, in that $Si_xO_yN_z$ and Al_xO_y appear to be more

resistant to SAC etch conditions than is a silicon nitride protective material. However, the materials of U.S. Pat. No. 5,700,349 have problems associated with their use, and it would be desirable to overcome such problems.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming an insulative material along a conductive structure. A conductive structure is provided over a substrate, and an electrically insulative material is formed along at least a portion of the conductive structure. The electrically insulative material comprises at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10. A dopant barrier layer is formed over the electrically insulative material. BPSG is formed over the dopant barrier layer, and the dopant barrier layer prevents dopant migration from the BPSG to the electrically insulative material.

In another aspect, the invention encompasses methods of forming transistor structures.

In yet another aspect, the invention encompasses a transistor structure which includes a transistor gate formed over a semiconductive substrate. The transistor gate has a sidewall which comprises electrically conductive material. Source/drain regions are within the substrate and proximate the transistor gate. An electrically insulative material is along

the electrically conductive material of the sidewall of the transistor gate. The electrically insulative material comprises at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10. A layer consisting of silicon dioxide is over the transistor gate, electrically insulative material and substrate. A layer of BPSG is over the layer consisting of silicon dioxide.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a portion of a semiconductor wafer at an initial processing step of a method of the present invention.

Fig. 2 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 1 in accordance with a second embodiment of the present invention.

Fig. 7 is a view of the Fig. 6 wafer fragment shown at a processing step subsequent to that of Fig. 6.

Fig. 8 is a view of the Fig. 6 wafer fragment shown at a processing step subsequent to that of Fig. 7.

Fig. 9 is a view of the Fig. 6 wafer fragment shown at a processing step subsequent to that of Fig. 8.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In one aspect, the invention is a recognition that deposited antireflective coating (DARC) materials (which are typically $Si_xO_yN_z$, wherein x, y and z are greater than 0 and less than 10) can be utilized to protect conductive materials of wordlines during an etch of BPSG (such as, for example, during a SAC etch).

The invention also encompasses a recognition that if $Si_xO_yN_z$ is utilized to protect a conductive material during an etch, the $Si_xO_yN_z$ is preferably electrically insulative. The $Si_xO_yN_z$ can then function to

prevent shorting between the protected conductive material and other conductive materials proximate the protected conductive material.

Further, the invention encompasses a recognition that $Si_xO_yN_z$ can have different characteristics if dopant is provided therein relative to if the material is undoped. Specifically, if dopant permeates within $Si_xO_yN_z$, the material can develop conductive characteristics which will destroy its ability to function as an electrically insulative protective layer. Dopant can migrate from a doped oxide (such as, for example, BPSG) provided against $Si_xO_yN_z$, and accordingly the invention encompasses provision of a dopant barrier layer between $Si_xO_yN_z$ and a doped oxide provided proximate the $Si_xO_yN_z$.

Dopant migration problems may also occur relative to materials comprising Al_pO_q (wherein p and q are greater than 0 and less than 10), and accordingly the invention also comprises provision of a dopant barrier layer between materials comprising Al_pO_q and doped oxide (such as, for example, BPSG).

A first embodiment method of the present invention is described with reference to Figs. 1-5. Referring initially to Fig. 1, a semiconductor wafer fragment 10 comprises a semiconductive material substrate 12 having wordlines 14, 16, 18 and 20 formed thereover. Substrate 12 can comprise, for example, monocrystalline silicon lightly doped with a background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and

"semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Wordlines 14, 16, 18 and 20 comprise a gate oxide layer 22, a polysilicon layer 24, a silicide layer 26, a silicon dioxide layer 28, and an insulative cap 30. Gate oxide layer 22 can comprise, for example, silicon dioxide; semiconductive material layer 24 can comprise, for example, conductively-doped polysilicon; silicide layer 26 can comprise, for example, tungsten silicide or titanium silicide; and insulative cap 30 can comprise, for example, silicon nitride.

Shallow trench isolation regions 32 are formed within substrate 12 and electrically isolate at least some of the shown electrical components of wafer fragment 10 from adjacent circuitry (not shown).

Conductively doped diffusion regions 34, 36 and 38 are formed within substrate 12 and between wordlines 14, 16, 18 and 20. Wordlines 14, 16, 18 and 20 extend into and out of the page (i.e., are in the shape of lines extending across a top of substrate 12), and paired diffusion regions are formed within substrate 12 at spaced intervals along the wordlines. The portions of the wordlines which gatedly connect pairs

of diffusion regions constitute transistor gates. Accordingly, the shown portion of wordline 16 constitutes a transistor gate between diffusion regions 34 and 36, and the shown portion of wordline 18 constitutes a transistor gate between diffusion regions 36 and 38.

Diffusion regions 34, 36 and 38 can be doped with one or both of n-type dopant and p-type dopant, and can comprise halo regions and/or lightly doped diffusion (Ldd) regions for transistor structures formed from gates 16 and 18.

Wordlines 14, 16, 18 and 20 comprise sidewalls 15, 17, 19 and 21, respectively, with portions of the sidewalls defined by layers 24 and 26 comprising conductive portions. A silicon dioxide layer 40 is formed along the conductive portions of sidewalls 15, 17, 19 and 21, as well as over diffusion regions 34, 36 and 38. Silicon dioxide layer 40 can be formed by, for example, exposing wafer fragment 10 to oxidizing conditions. Such oxidation can correspond to so-called "smiling gate" oxidation which is known in the art to improve performance of transistor devices. In particular embodiments of the invention which are not shown, layer 40 can be eliminated (e.g., not formed).

Referring to Fig. 2, a pair of layers 42 and 44 are formed over wordlines 14, 16, 18 and 20, as well as over regions of substrate 12 between wordline 14, 16, 18 and 20. Layers 42 and 44 comprise electrically insulative material, and at least one of layers 42 and 44 comprises at least one of $Si_xO_yN_z$ (silicon oxynitride) and Al_pO_q, with p,

q, x, y and z being greater than 0 and less than 10. Layers 42 and 44 can further comprise other insulative materials such as, for example, silicon nitride (which typically is Si_3N_4). Each of layers 42 and 44 can have a thickness of, for example, from about 10Å to about 750Å, with a suitable thickness being about 150Å. In embodiments in which layer 40 is not formed (not shown), layer 42 will physically contact (i.e., be against) the conductive material of wordlines 14, 16, 18 and 20.

In particular embodiments, one of layers 42 and 44 can consist of either $Si_xO_yN_z$ or Al_pO_q (or consist essentially of such materials), and the other of layers 42 and 44 can consist of silicon and nitrogen (or consist essentially of silicon and nitrogen), and can be, for example, Si_3N_4. Alternatively, one of layers 42 and 44 can consist of aluminum and oxygen (or consist essentially of such materials), and the other of layers 42 and 44 can consist of silicon and nitrogen (or consist essentially of such materials). In yet another alternative embodiment, one of layers 42 and 44 can consist of silicon, nitrogen and oxygen (or consist essentially of such materials), and the other of layers 42 and 44 can consist of silicon and nitrogen (or consist essentially of such materials). An exemplary material which consists of aluminum and oxygen Al_2O_3.

Referring to Fig. 3, layers 42 and 44 are anisotropically etched to form electrically insulative pillars 45, 47, 49 and 51 along sidewalls 15, 17, 19 and 21, respectively. A suitable anisotropic etch of materials 42 and 44 can comprise, for example, a plasma etch utilizing one or more

of CF_4, CHF_3 and O_2. The anisotropic etch of layers 42 and 44 removes such layers from over wordlines 14, 16, 18 and 20.

Although in the shown embodiment pillars 45, 47, 49 and 51 are spaced from conductive portions of sidewalls 15, 17, 19 and 21 by silicon oxide layer 40, it is to be understood that the invention encompasses other embodiments (not shown) wherein oxide material 40 is not formed, and accordingly wherein pillars 45, 47, 49 and 51 are formed against the conductive portions of sidewalls 15, 17, 19 and 21. Also, although in the shown embodiment the anisotropic etching of materials 42 and 44 is selective relative to the silicon oxide material 40 such that oxide material 40 is not etched by the anisotropic etching conditions, it is to be understood that the invention encompasses other embodiments (not shown) wherein oxide material 40 is removed by the anisotropic etching conditions. Additionally, the invention encompasses embodiments in which oxide material 40 is removed in an etch subsequent to the anisotropic etch of materials 42 and 44.

Heavily doped source/drain regions 50, 52 and 54 are implanted proximate gates 16 and 18, utilizing pillars 45, 47, 49 and 51 as spacers to align the implants. Regions 50, 52 and 54 are referred to as "heavily doped" regions because they are more heavily doped than regions 34, 36 and 38. A typical peak dopant concentration in regions 50, 52 and 54 is greater than 10^{19} atoms/cm^3. The implanted dopant utilized to form heavily doped source/drain regions 50, 52 and 54 can be either p-type

dopant or n-type dopant, depending on whether PMOS or NMOS transistors are formed. It is noted that materials 42 and 44 do not extend over heavily-doped source/drain regions 50, 52 and 54.

Although source/drain regions 50, 52 and 54 are shown implanted through silicon oxide layer 40, it is to be understood that the invention encompasses other embodiments (not shown) wherein silicon oxide layer 40 is removed prior to the implant of regions 50, 52 and 54.

Referring to Fig. 4, a dopant barrier layer 60 is formed over pillars 45, 47, 49 and 51, as well as over wordlines 14, 16, 18 and 20. Dopant barrier layer 60 can consist of silicon dioxide (or consist essentially of silicon dioxide), and can be formed by chemical vapor deposition utilizing tetraethyl orthosilicate (TEOS) as a precursor. Layer 60 can comprise a thickness of, for example, about 250Å.

A doped oxide layer 62 is formed over dopant barrier layer 60, and can comprise, for example, BPSG. Dopant barrier layer 60 prevents dopant migration from doped oxide 62 into the $Si_xO_yN_z$ or Al_pO_q materials of pillars 45, 47, 49 and 51. Barrier layer 60 thus alleviates problems associated with dopant migrating into such materials and changing the properties of such materials from electrically insulative to electrically conductive.

Referring to Fig. 5, contact openings 66, 68 and 70 are etched through layers 60 and 62 to expose upper surfaces of source/drain regions 50, 52 and 54. Openings 66, 68 and 70 can be formed by

photolithographic processing (i.e., by providing a patterned layer of photoresist over an upper surface of doped oxide 62, and subsequent etching through oxides 40, 60 and 62), or other techniques. Pillars 45, 47, 49 and 51 are utilized to align bottom portions of openings 66, 68 and 70 relative to source/drain regions 50, 52 and 54, and accordingly the formation of openings 66, 68 and 70 constitutes a SAC etch. The $Si_xO_yN_z$ and/or Al_pO_q of pillars 45, 47, 49 and 51 reduces etching of the pillars relative to that which would occur if the pillars were formed entirely of Si_3N_4. However, as discussed above with reference to Fig. 2, one of layers 42 and 44 can consist essentially of silicon nitride. It can be advantageous to have the innermost of the layers (i.e., layer 42) consist of either $Si_xO_yN_z$ or Al_pO_q, and the outermost of the layers (i.e., layer 44) consist of silicon nitride, so that if there is some over-etching occurring during the anisotropic etching described with reference to Fig. 3, it will be silicon nitride layer 44 which is removed, rather than the layer of $Si_xO_yN_z$ or Al_pO_q.

Conductive material 72 is formed within openings 66, 68 and 70 to form electrical contacts to source/drain regions 50, 52 and 54. Conductive material 72 can comprise conductively-doped polysilicon, and/or metal, and can comprise multiple materials, such as, for example, a silicide at a lower portion where it joins the source/drain region and either metal nitride or metal above the silicide. In the shown embodiment, wafer fragment 10 comprises a planarized upper surface 74

which can be formed by, for example, chemical-mechanical planarization after filling openings 66, 68 and 70 with conductive material 72.

Another embodiment of the invention is described with reference to Figs. 6-9. In referring to Figs. 6-9, similar numbering will be utilized as was used above in describing Figs. 1-5, where appropriate.

Referring first to Fig. 6, a wafer fragment 100 comprises a substrate 12 having wordlines 14, 16, 18 and 20 formed thereover. An insulative material 102 is provided over wordlines 14, 16, 18 and 20, as well as over regions of substrate 12 between wordlines 14, 16, 18 and 20. Material 102 consists of, or consists essentially of, $Si_xO_yN_z$ or Al_pO_q, with p, q, x, y and z being greater than 0 and less than 10, and can be provided to a thickness of, for example, from about 10Å to about 750Å, with a suitable thickness being greater than about 50Å, and being, for example, about 25% of the gate length for the particular structure. In embodiments in which layer 40 is not formed (not shown), material 102 will contact conductive material of gates 14, 16, 18 and 20.

Referring to Fig. 7, material 102 is anisotropically etched to form insulative pillars 104, 106, 108 and 110 adjacent wordlines 14, 16, 18 and 20, respectively. Subsequently, source/drain regions 50, 52 and 54 are implanted into substrate 12.

Referring to Fig. 8, a dopant barrier layer 60 and doped oxide layer 62 are provided over wordlines 14, 16, 18 and 20 as well as over pillars 104, 106, 108 and 110.

Referring to Fig. 9, openings 66, 68 and 70 are formed through materials 40, 60 and 62 to source/drain regions 50, 52 and 54, and such openings are filled with conductive material 72. The formation of openings 66, 68 and 70 can be accomplished by the processing described above with reference to Fig. 5, and accordingly can constitute a SAC etch. Pillars 104, 106, 108 and 110 protect conductive material of wordlines 14, 16, 18 and 20 from being etched during the formation of openings 66, 68 and 70. Further, protective layer 60 (which, as described above, can consist of silicon dioxide and be chemical vapor deposited utilizing TEOS as a precursor), prevents dopant migration from doped oxide 62 into the material of pillars 104, 106, 108 and 110.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming an insulative material along a conductive structure, comprising:

providing a conductive structure over a substrate;

forming an electrically insulative material along at least a portion of the conductive structure, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

forming a dopant barrier layer over the electrically insulative material; and

forming a doped oxide material over the dopant barrier layer, the dopant barrier layer preventing dopant migration from the doped oxide material to the electrically insulative material.

2. The method of claim 1 wherein the electrically insulative material is formed to a thickness of at least about 50Å.

3. The method of claim 1 wherein the electrically insulative material consists essentially of the $Si_xO_yN_z$.

4. The method of claim 1 wherein the electrically insulative material consists essentially of the $Si_xO_yN_z$ and is against the conductive structure.

5. The method of claim 1 wherein the electrically insulative material consists essentially of the Al_pO_q.

6. The method of claim 1 wherein the electrically insulative material consists essentially of the Al_pO_q and is against the conductive structure.

7. The method of claim 1 wherein the forming the dopant barrier layer comprises chemical vapor depositing silicon oxide from a TEOS precursor.

8. The method of claim 1 wherein the doped oxide material comprises BPSG.

9. A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall; the electrically insulative material comprising at least two separate layers; the at least two layers having different chemical compositions from one another; a first of the at least two layers comprising at least one of $Si_xO_yN_z$ or Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10; a second of the at least two layers consisting essentially of silicon and nitrogen; and

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall; the anisotropically etching comprising etching both of the first and second of the at least two layers.

10. The method of claim 9 further comprising implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant.

11. The method of claim 9 wherein the first of the at least two layers is between the second of the at least two layers and the transistor gate sidewall.

12. The method of claim 9 wherein the first of the at least two layers consists essentially of the $Si_xO_yN_z$ and is between the second of the at least two layers and the transistor gate sidewall.

13. The method of claim 9 wherein the first of the at least two layers consists essentially of the Al_pO_q and is between the second of the at least two layers and the transistor gate sidewall.

14. A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming source/drain regions within the substrate and proximate the transistor gate;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

chemical vapor depositing silicon oxide over the transistor gate and electrically conductive material utilizing a TEOS precursor; and

forming BPSG over the silicon oxide, the BPSG being spaced from the electrically insulative material of the spacer by the silicon oxide.

15. The method of claim 14 wherein the electrically insulative material is formed to extend across a top of the transistor gate.

16. The method of claim 14 wherein the electrically insulative material consists of Al_2O_3.

17. The method of claim 14 wherein the electrically insulative material consists of aluminum and oxygen.

18. The method of claim 14 wherein the electrically insulative material consists of silicon, nitrogen and oxygen.

19. A method of forming a transistor structure, comprising:

forming a transistor gate over a substrate, the transistor gate comprising a sidewall which comprises electrically conductive material;

forming an electrically insulative material along the electrically conductive material of the transistor gate sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

anisotropically etching the electrically insulative material to form a spacer along the transistor gate sidewall;

implanting a dopant into the substrate and utilizing the spacer to align the dopant during the implant;

chemical vapor depositing silicon oxide over the transistor gate and spacer utilizing TEOS as a precursor of the silicon oxide; and

forming BPSG over the silicon oxide, the BPSG being spaced from the electrically insulative material of the spacer by the silicon oxide.

20. The method of claim 19 wherein the electrically insulative material comprises to different layers that are against one another, one of the layers consisting of silicon nitride, and the other of the two layers consisting of either the $Si_xO_yN_z$ or the Al_pO_q.

21. A transistor structure, comprising:

a semiconductive substrate;

a transistor gate over the substrate, the transistor gate having a sidewall which comprises electrically conductive material;

source/drain regions within the substrate and proximate the transistor gate;

an electrically insulative material along the electrically conductive material of the sidewall, the electrically insulative material comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

a layer consisting of silicon dioxide over the transistor gate, electrically insulative material, and substrate; and

a layer of BPSG over the layer consisting of silicon dioxide.

22. The structure of claim 21 wherein the electrically insulative material extends across a top of the transistor gate.

23. The structure of claim 21 wherein the electrically insulative material does not extend across a top of the transistor gate.

24. The structure of claim 21 wherein the electrically insulative material does not extend across a top of the source/drain regions.

25. The structure of claim 21 wherein the electrically insulative material consists of aluminum and oxygen.

26. The structure of claim 21 wherein the electrically insulative material consists of Al_2O_3.

27. The structure of claim 21 wherein the electrically insulative material consists of silicon, nitrogen and oxygen.

28. The structure of claim 21 wherein the electrically insulative material comprises a layer of silicon nitride against a layer of the $Si_xO_yN_z$.

29. The structure of claim 21 wherein the electrically insulative material comprises a layer of silicon nitride against a layer of the Al_pO_q.

30. A transistor structure, comprising:

a substrate;

a transistor gate over the substrate, the transistor gate having a sidewall which comprises electrically conductive material;

source/drain regions within the substrate and proximate the transistor gate;

an electrically insulative pillar along the electrically conductive material of the sidewall, the pillar comprising a first material against a second material, one of the first and second materials comprising at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10;

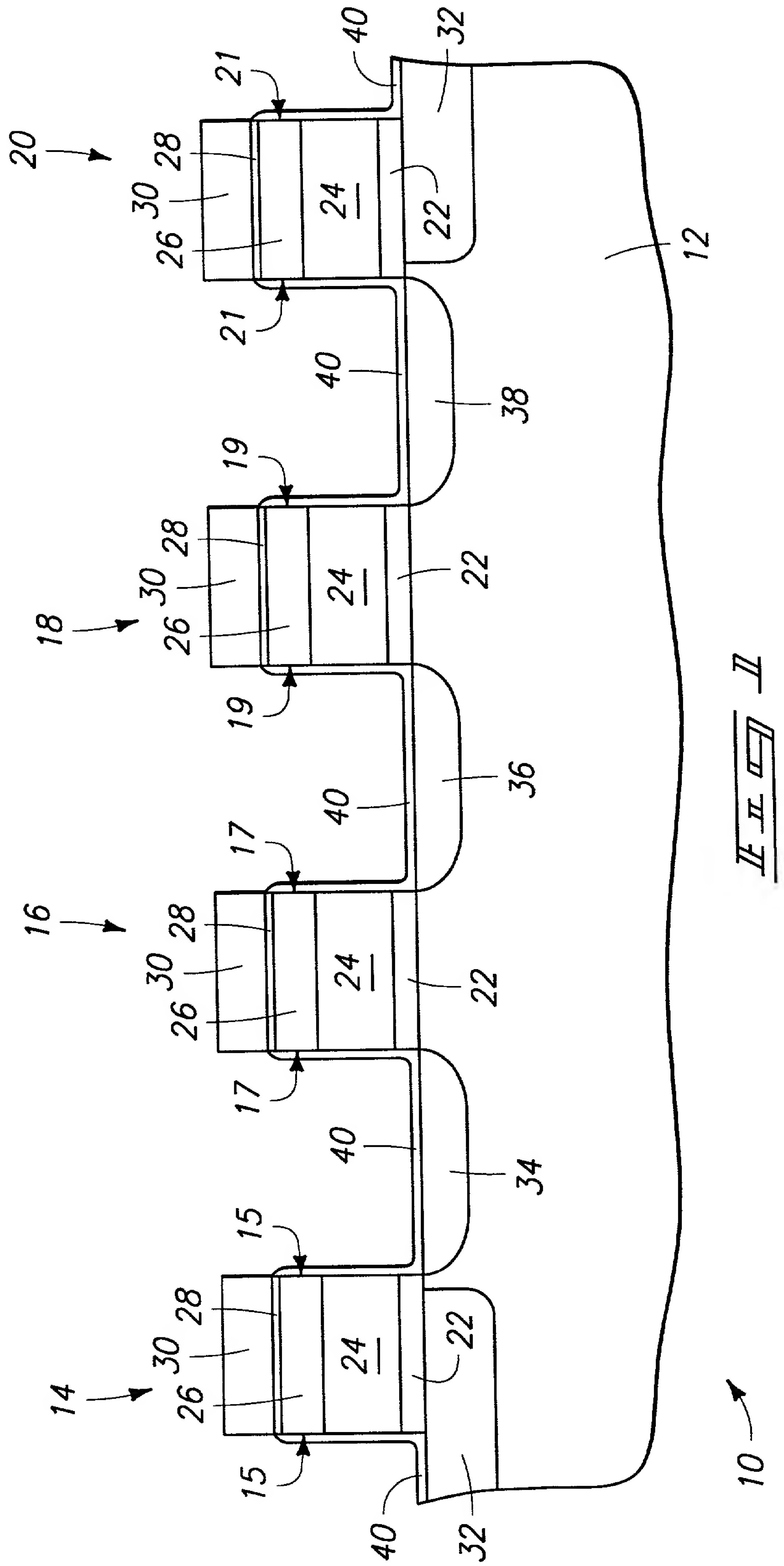
a layer consisting of silicon dioxide over the transistor gate, pillar and substrate; and

a layer of BPSG over the layer consisting of silicon dioxide.

31. The structure of claim 30 wherein the first material is silicon nitride and the second material is silicon oxynitride.

ABSTRACT OF THE DISCLOSURE

The invention encompasses a method of forming an insulative material along a conductive structure. A conductive structure is provided over a substrate, and an electrically insulative material is formed along at least a portion of the conductive structure. The electrically insulative material comprises at least one of $Si_xO_yN_z$ and Al_pO_q, wherein p, q, x, y and z are greater than 0 and less than 10. A dopant barrier layer is formed over the electrically insulative material. BPSG is formed over the dopant barrier layer, and the dopant barrier layer prevents dopant migration from the BPSG to the electrically insulative material. The invention also encompasses transistor structures, and methods of forming transistor structures.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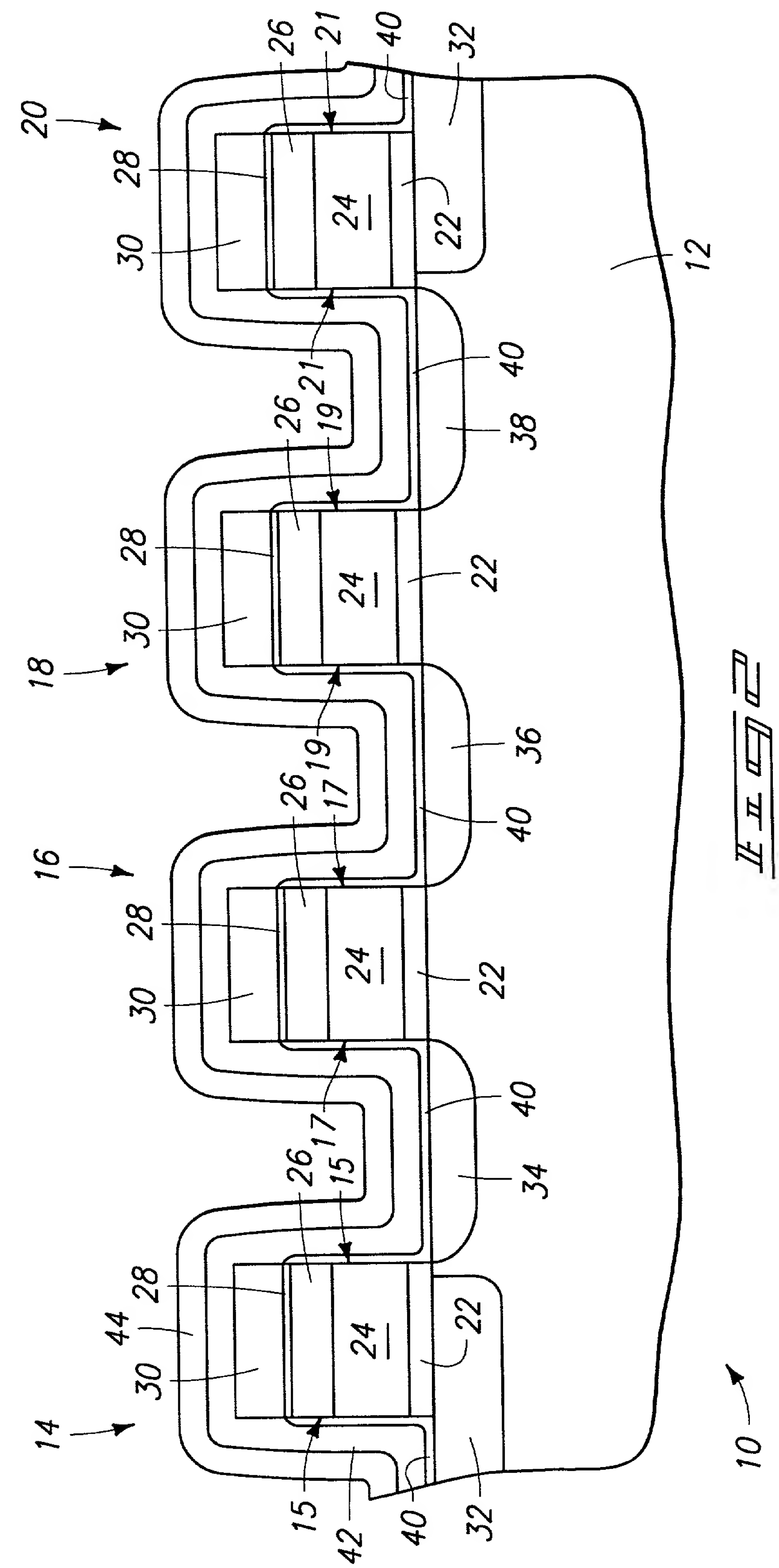
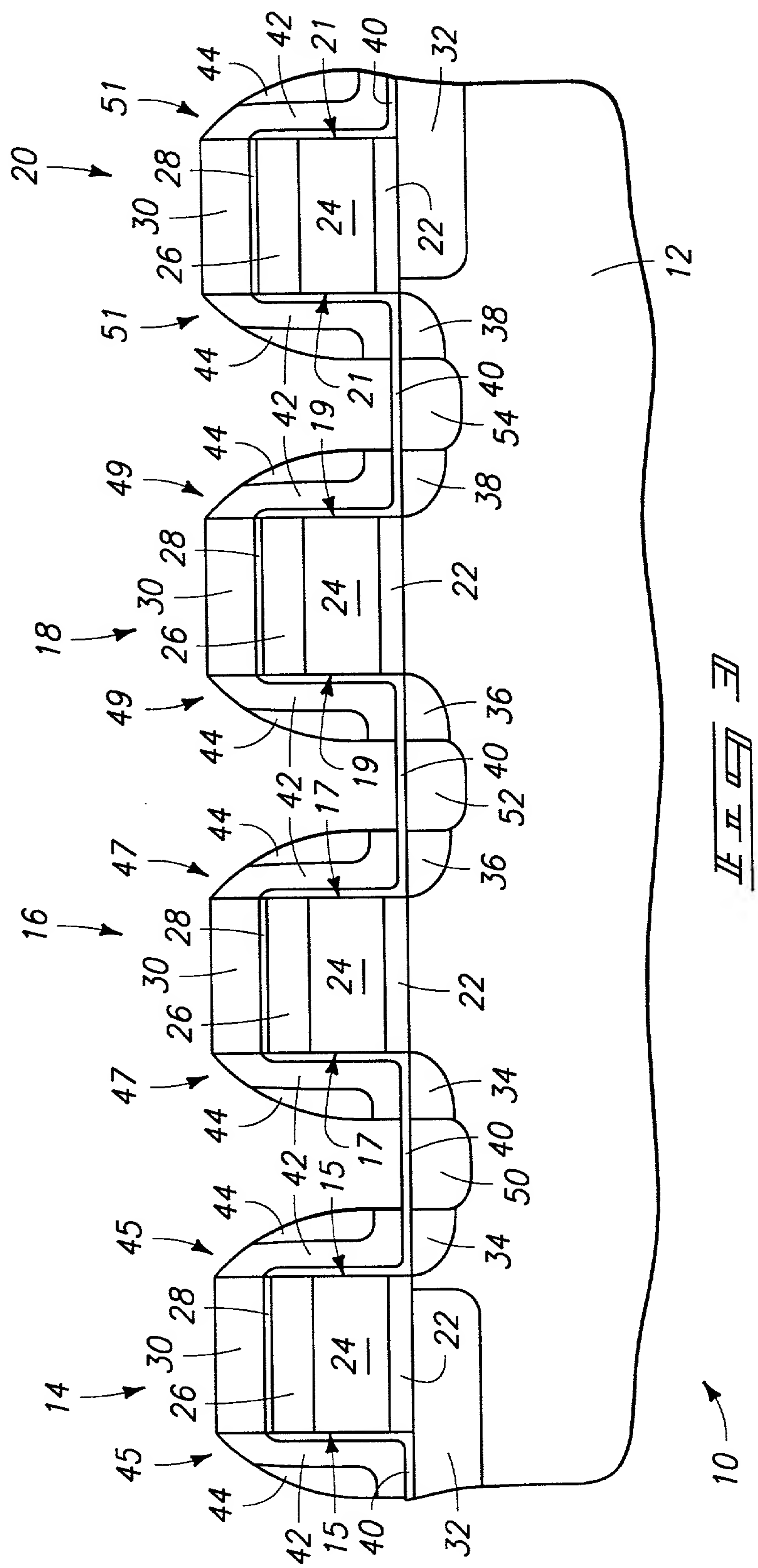


Fig. 2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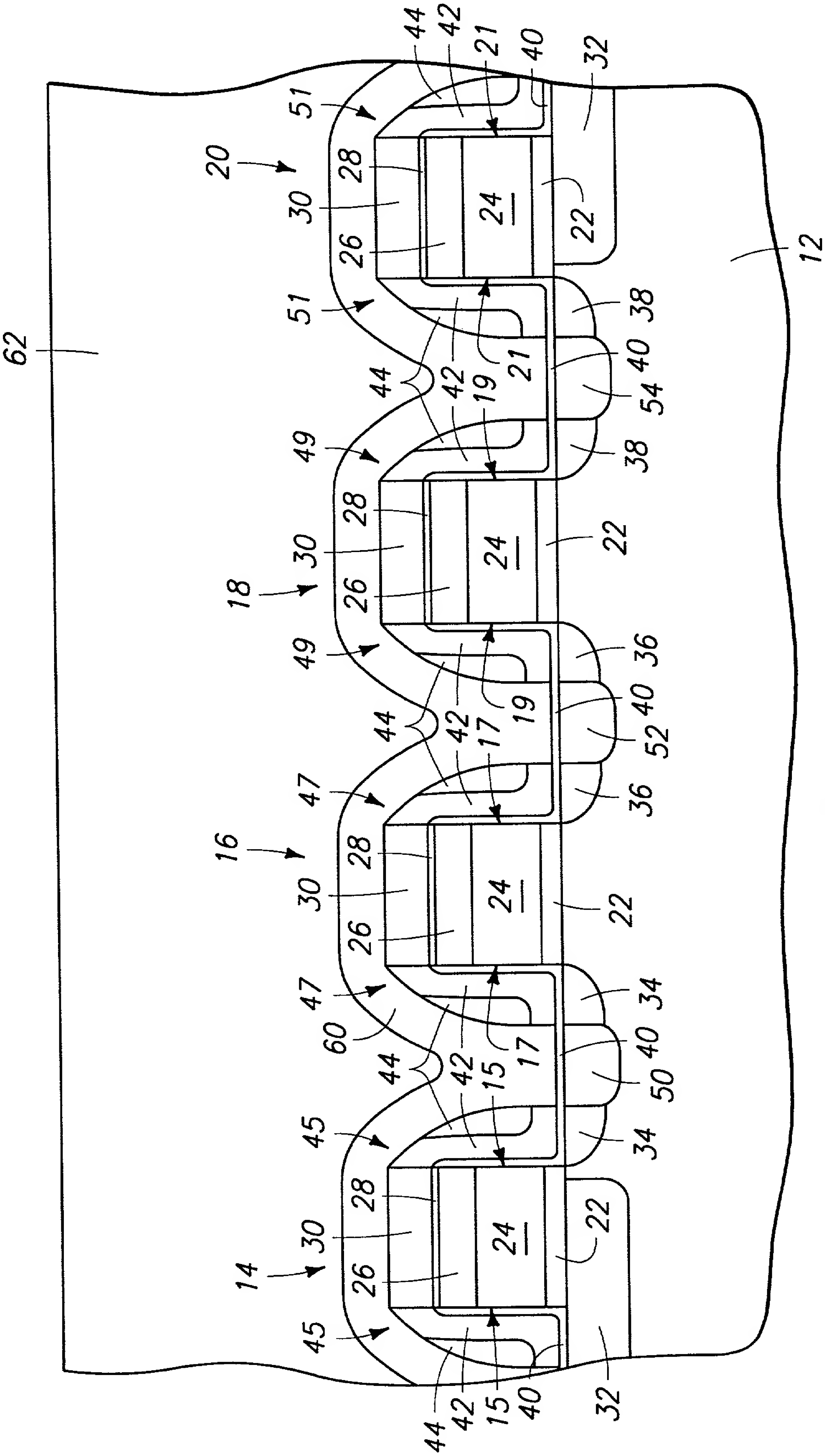
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Fig. 4

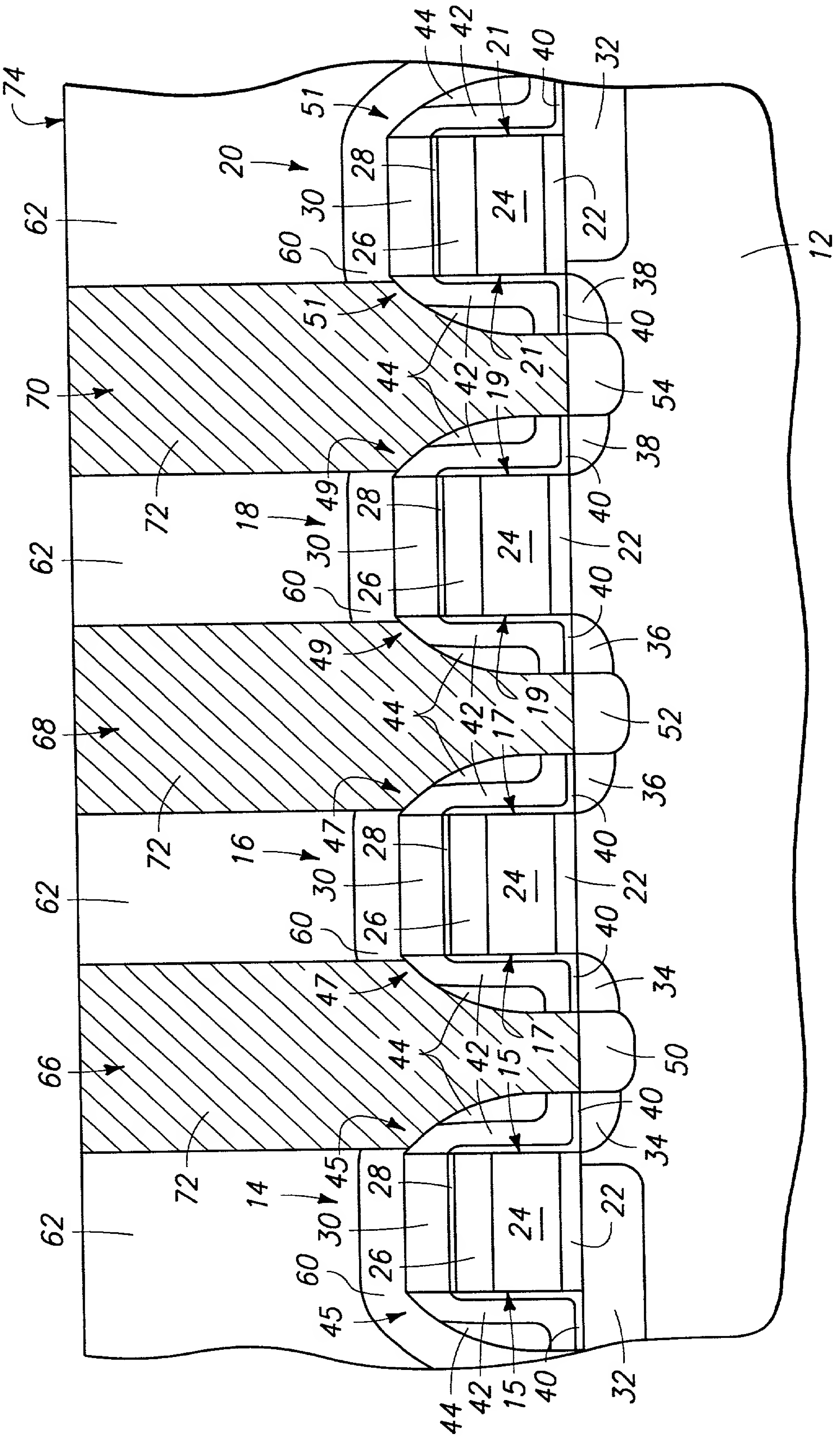

Fig. 5

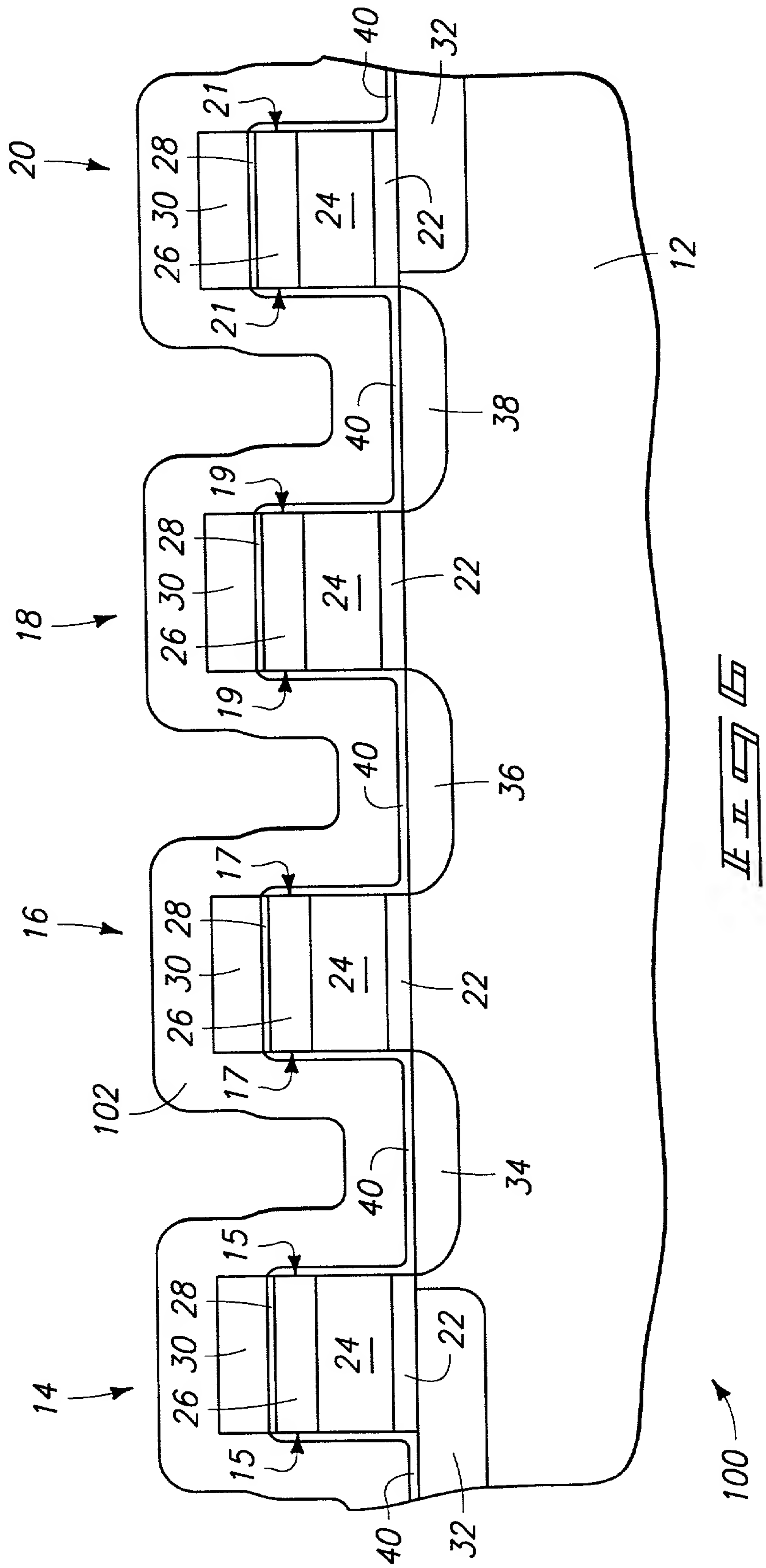
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FIG 6

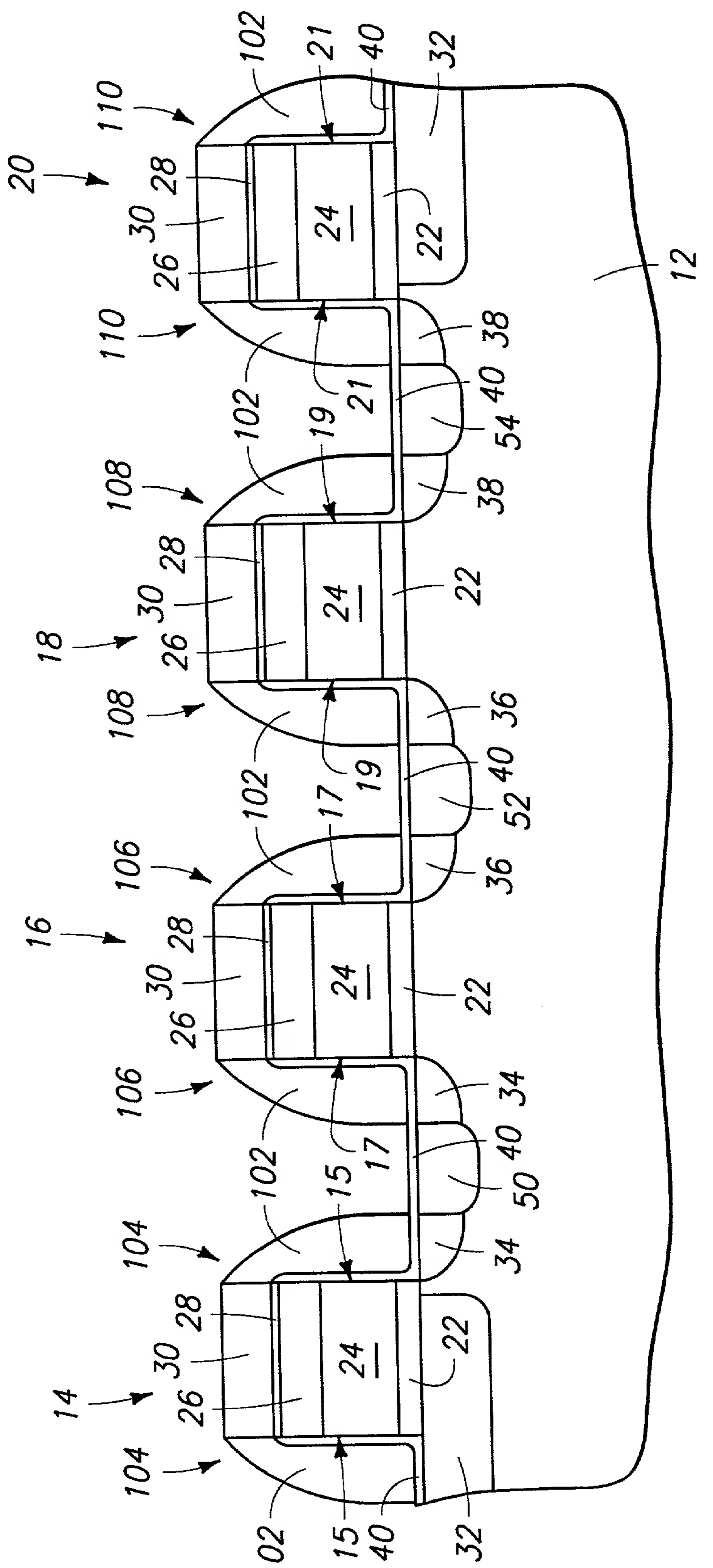
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Fig 7

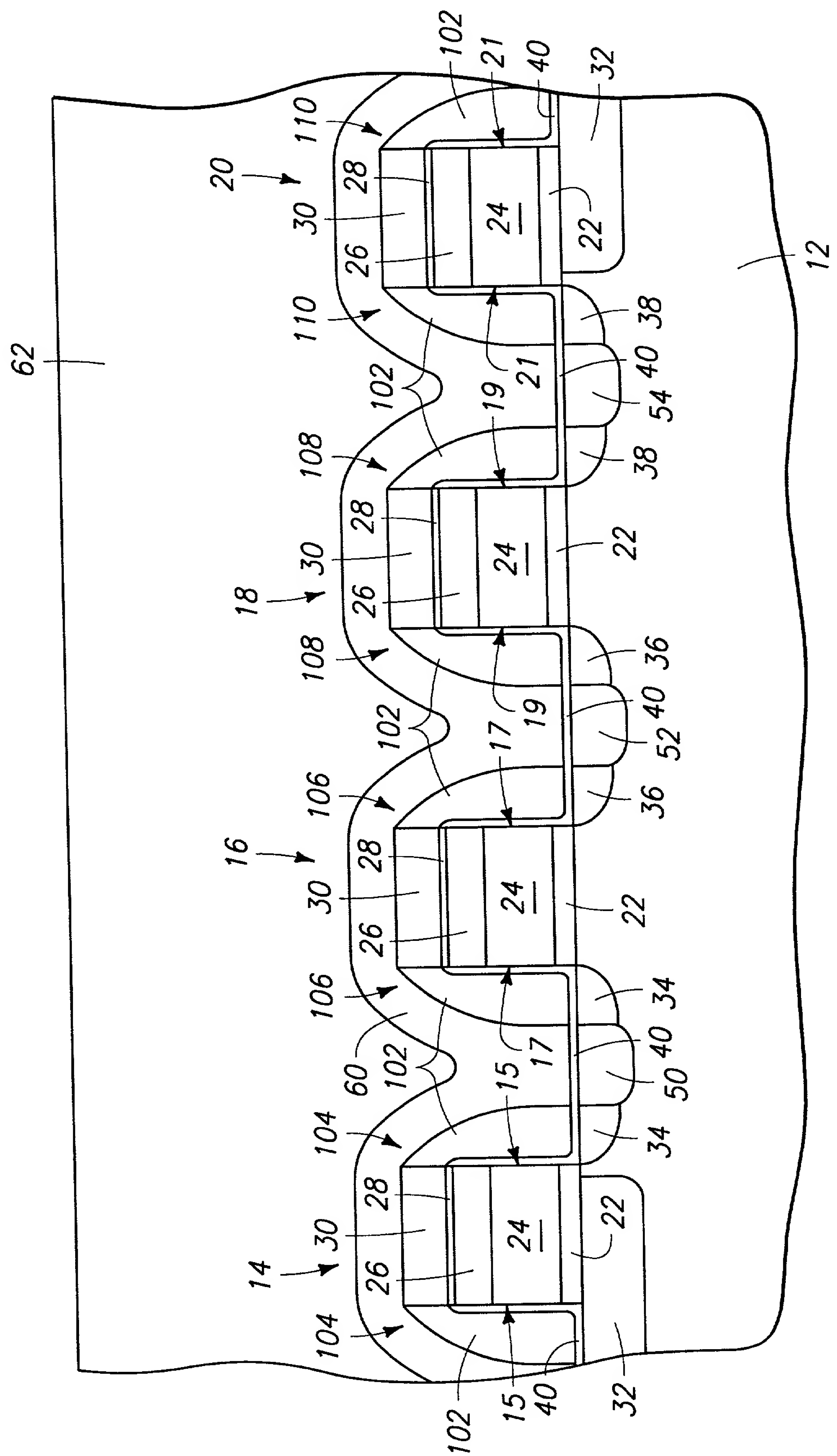

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Fig. 8

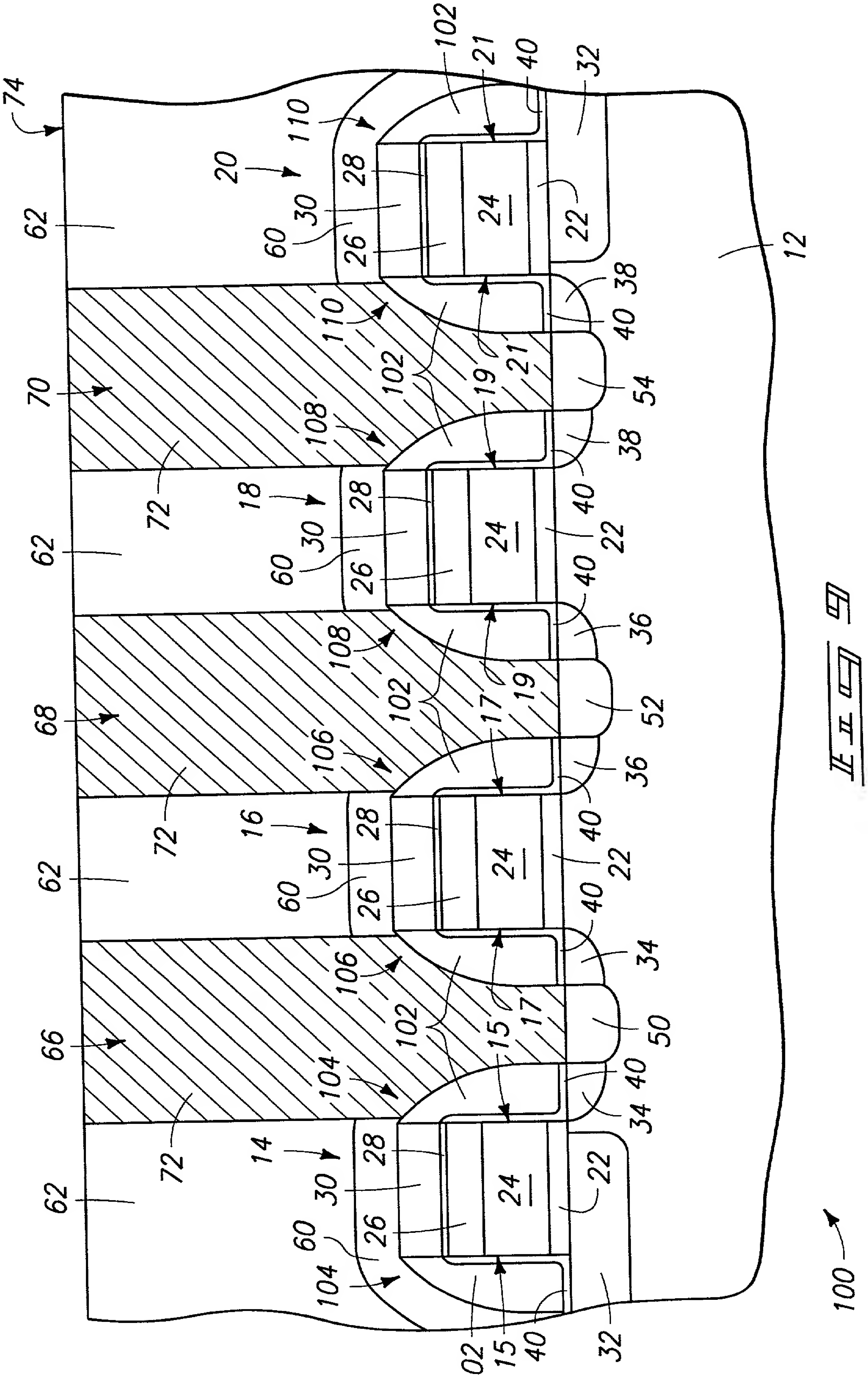
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FIG. 9

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DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Transistor Structures, Methods of Forming Transistor Structures, and Methods of Forming Insulative Material Against Conductive Structures, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so

made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

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